

FIG. 1

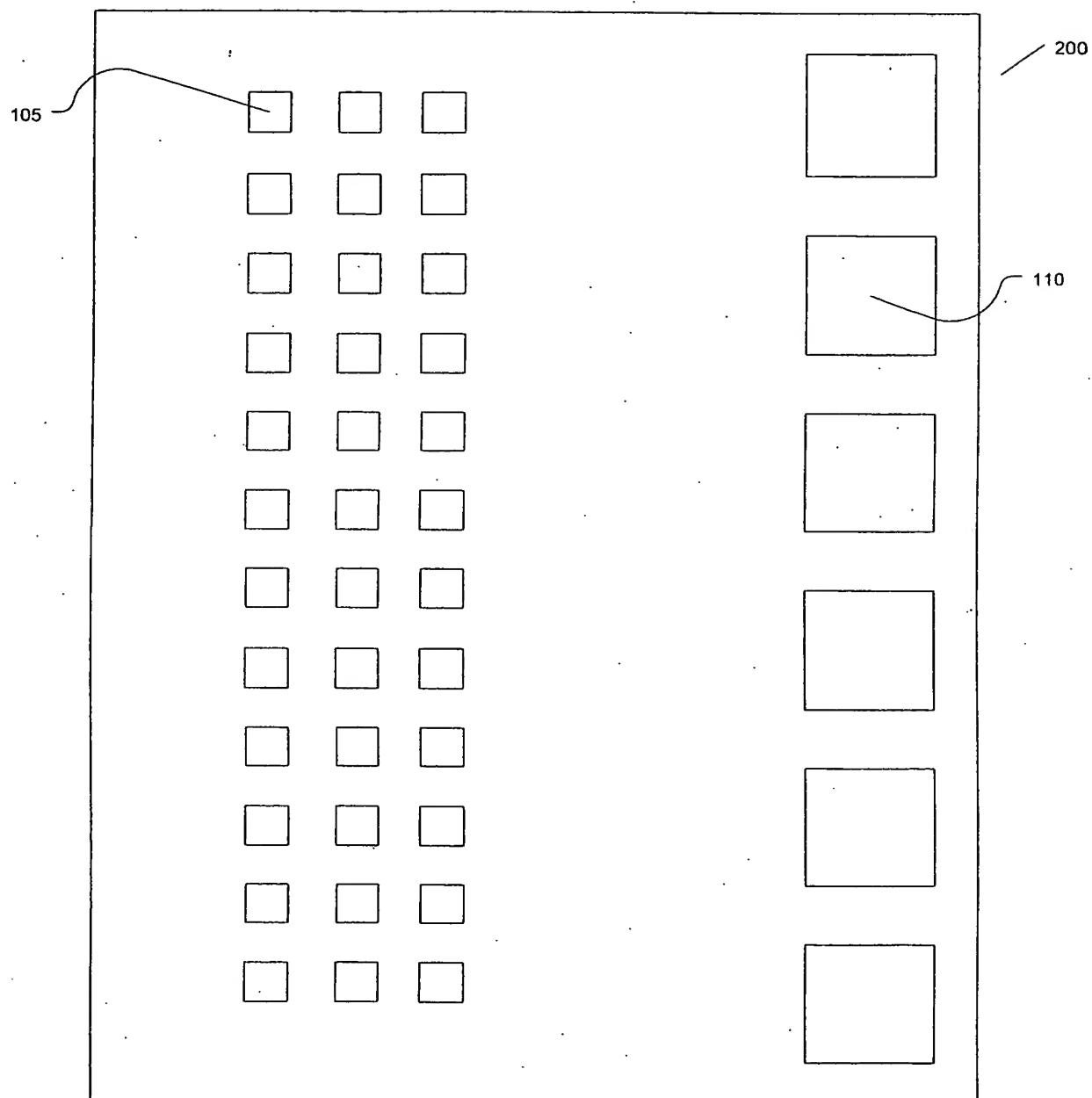


FIG. 2

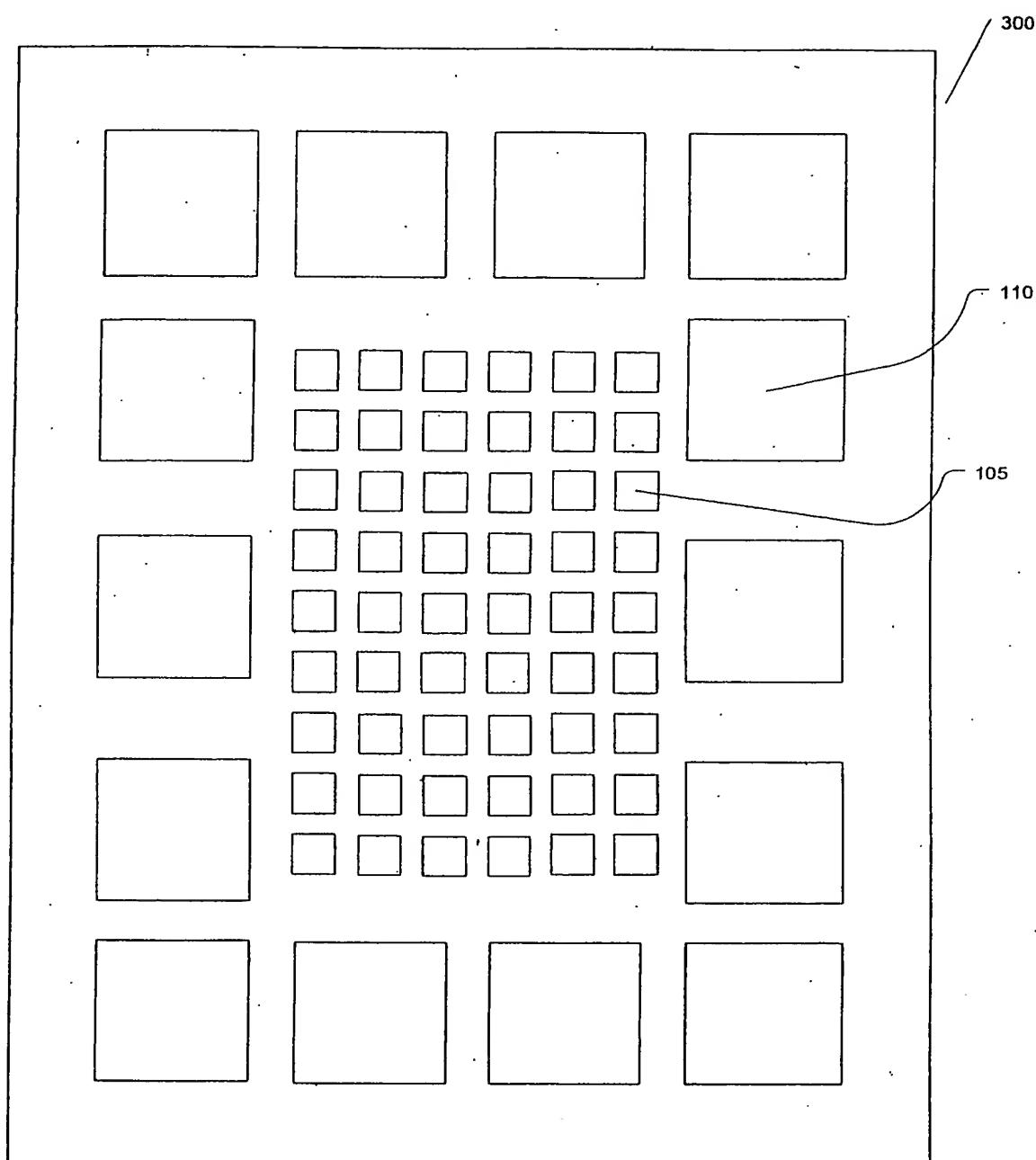


FIG. 3

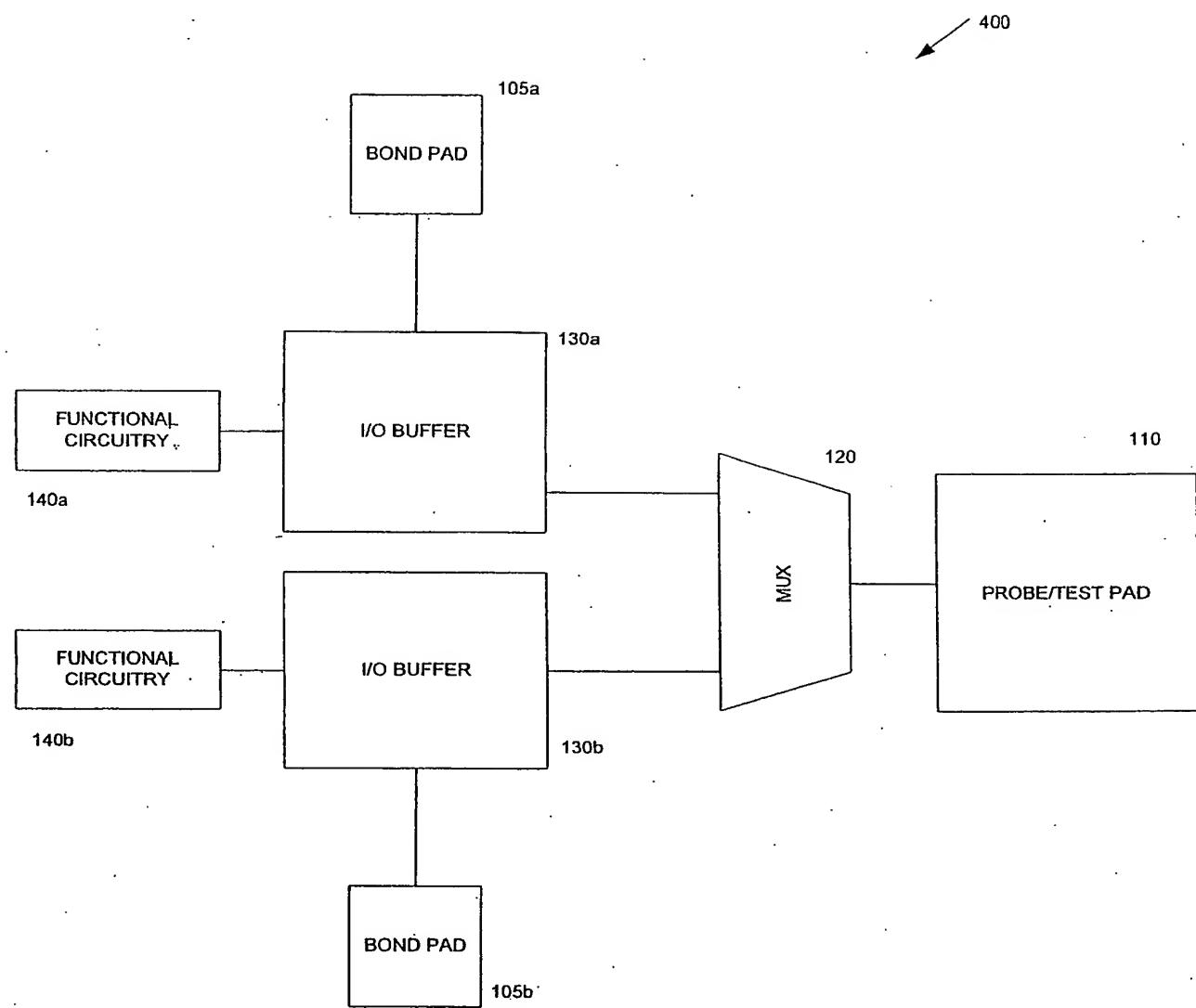


FIG. 4

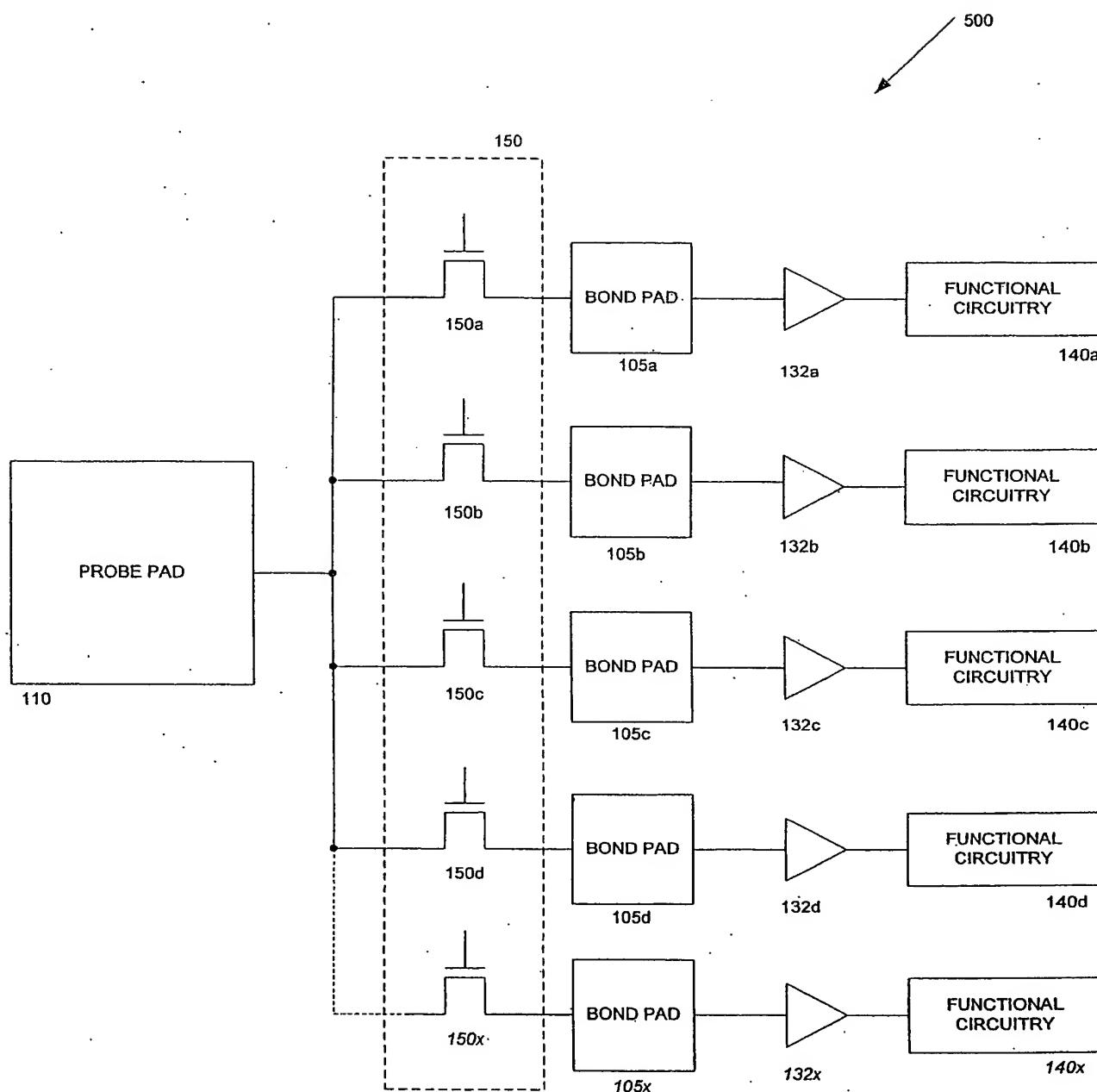


FIG. 5

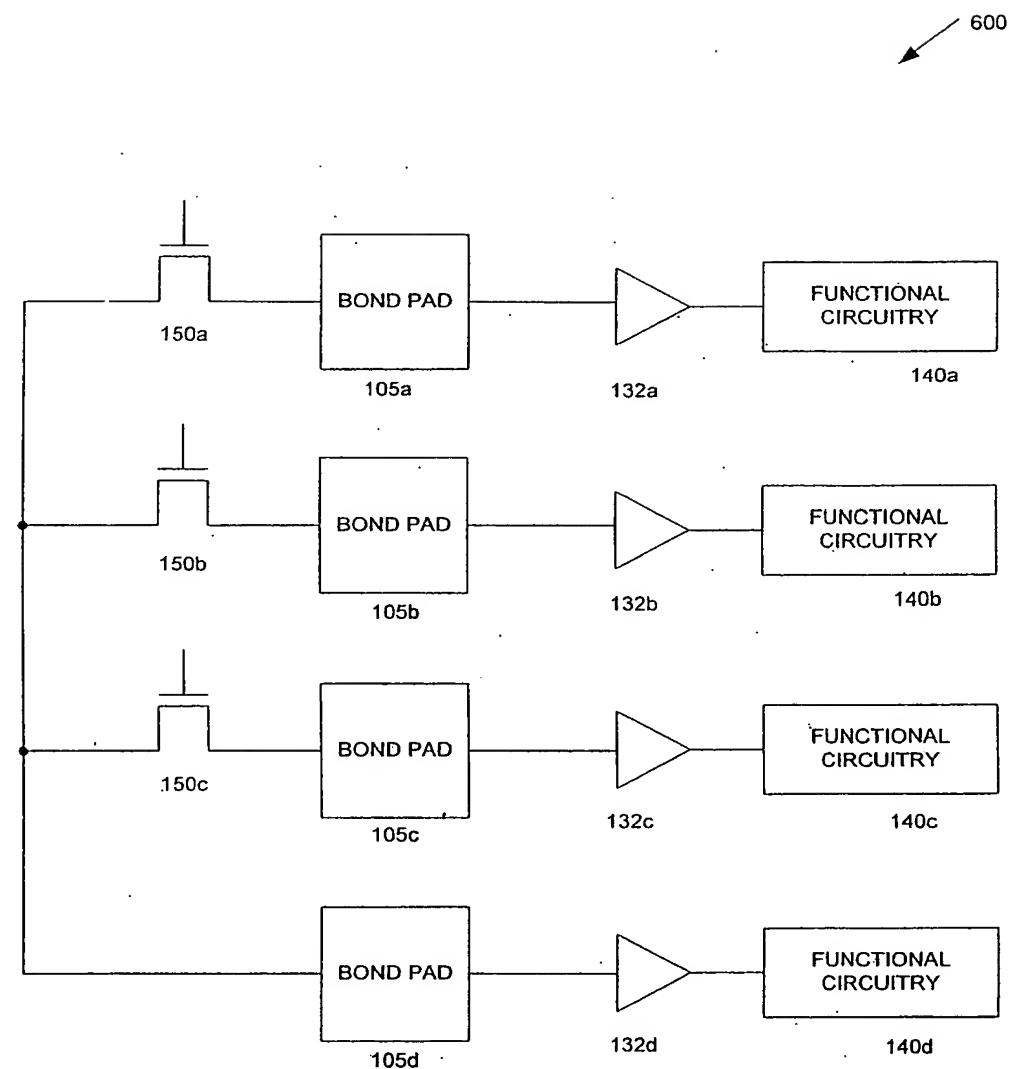


FIG. 6

"Layout and Use of Bond Pads and Probe Pads  
for Testing of Integrated Circuits Devices"

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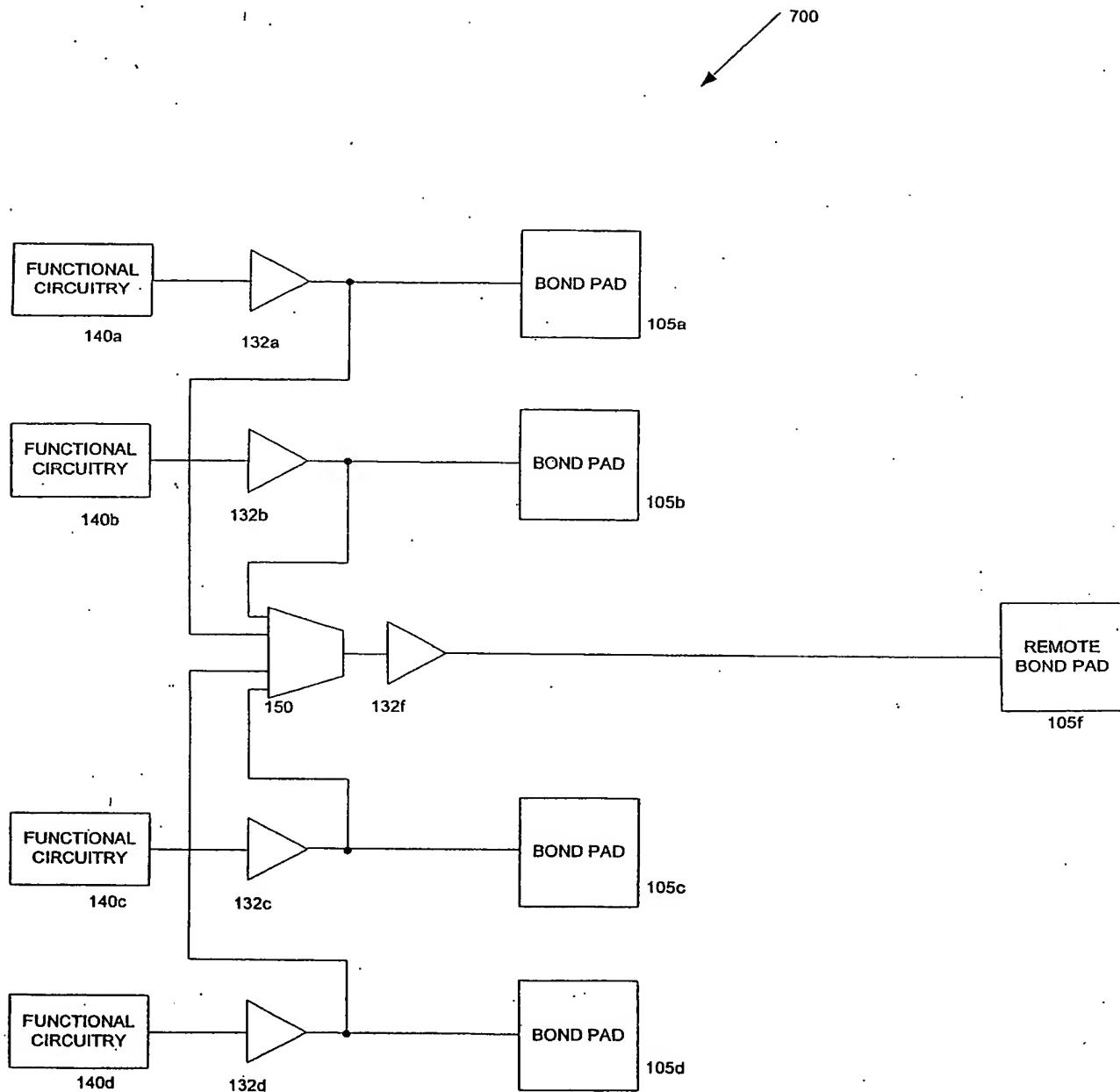


FIG. 7

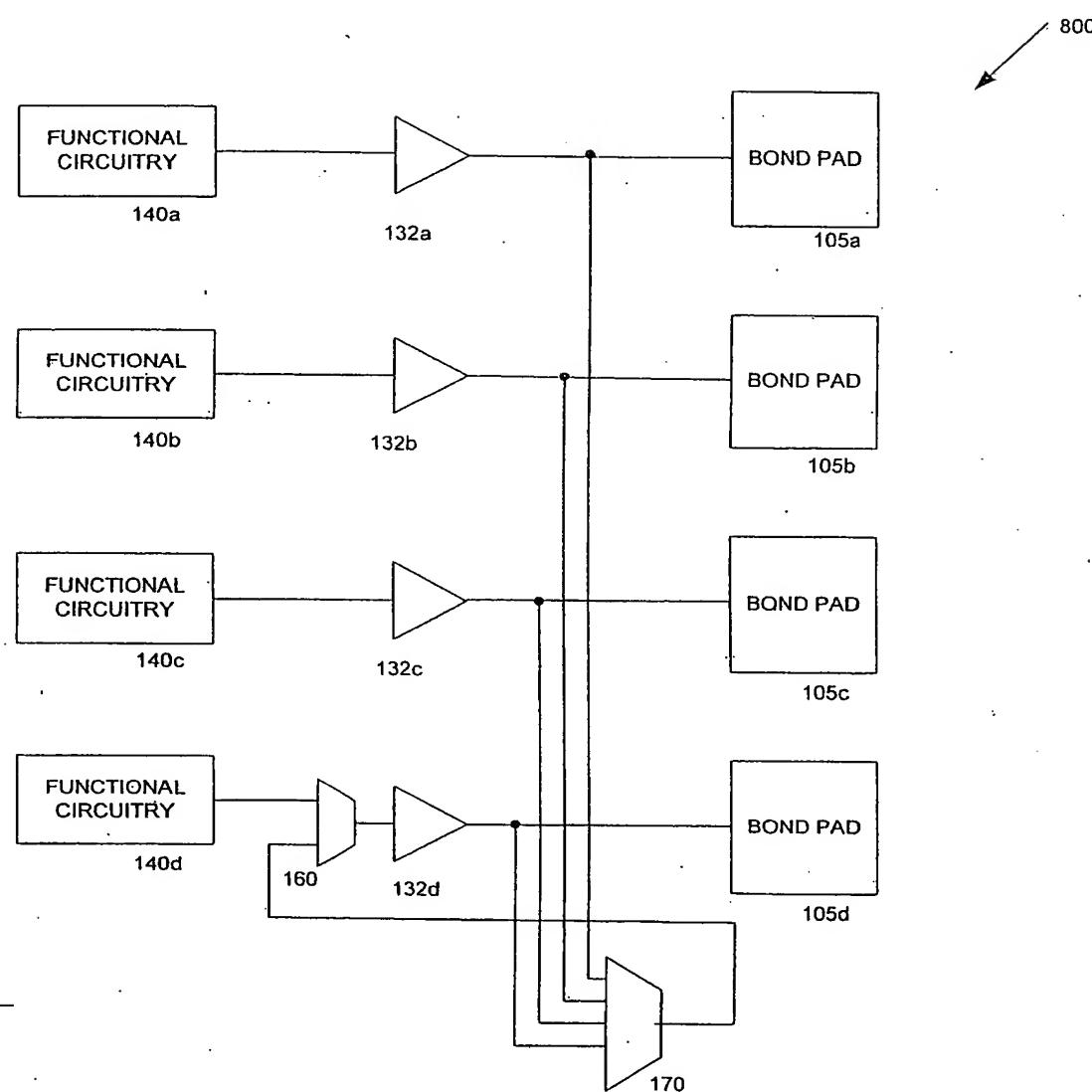


FIG. 8

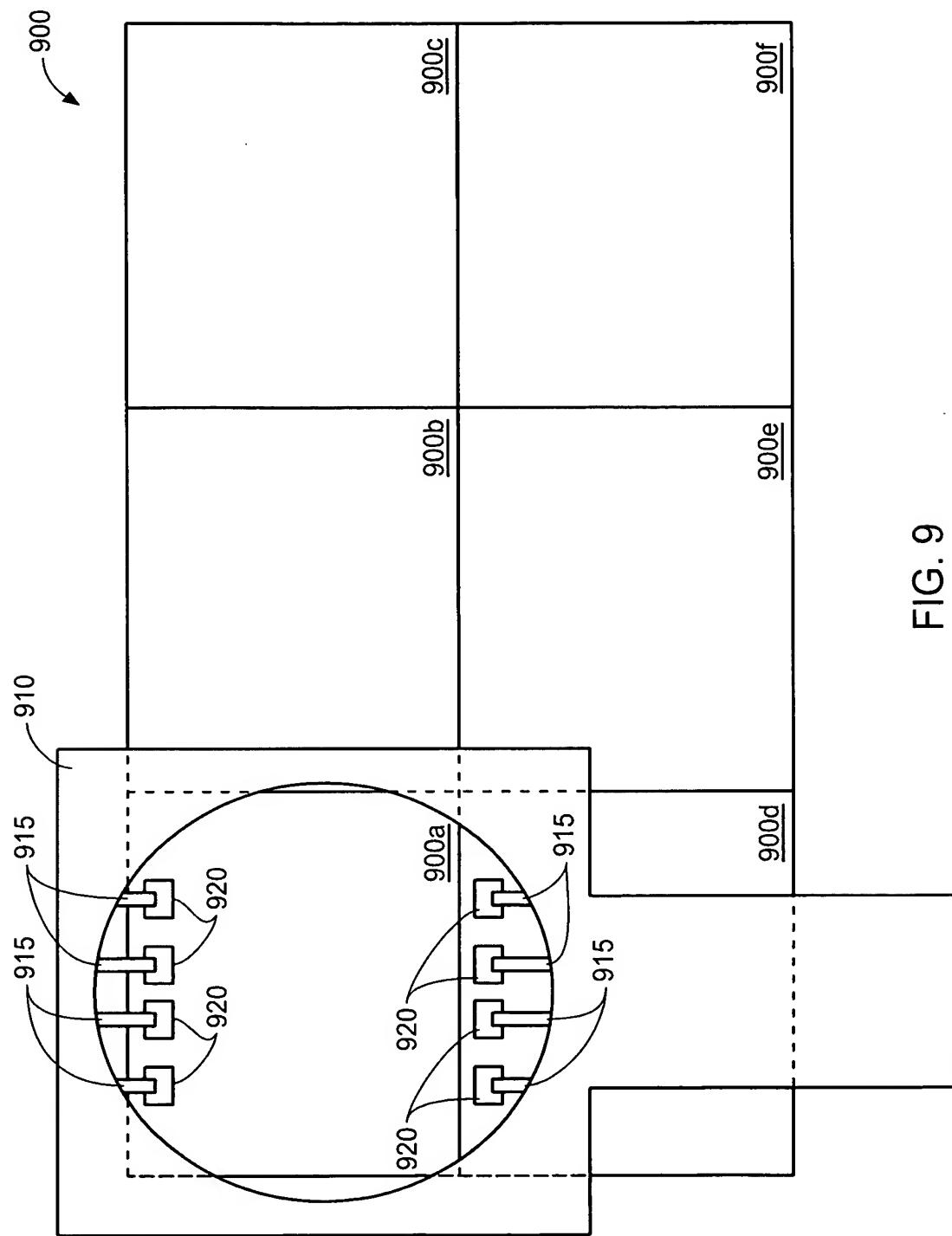


FIG. 9